PATENT ABSTRACTS OF JAPAN

(11)Publication number : **05-037305**

(43)Date of publication of application : **12.02.1993**

(51)Int.Cl. **H03K 3/037**

(21)Application number : **03-188619**

(22)Date of filing : **29.07.1991**

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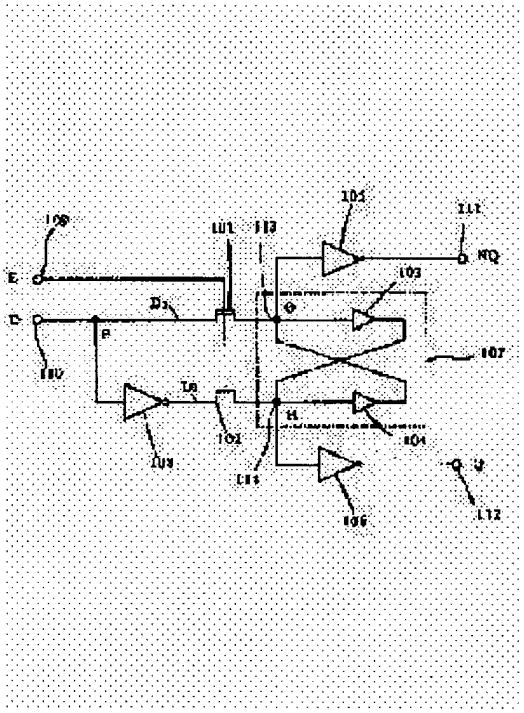
(54) LATCH CIRCUIT

(57)Abstract:

PURPOSE: To decrease a fluctuation of a delay time, and to execute a data transmission at a high speed by constituting a memory cell of an FF and execut ing a latch of data by both signals of forward tum and inversion, and designing an output inverter to a suitable size.

CONSTITUTION: When an enable signal E is inverted from 'L' to 'H' at the time TS1, NMOSTRs 101, 102 are turned on, and input data of 'H' is inputted to a G point through the TR 101. Simultaneously, data D2 inverted to 'L' is inputted through an output inverter 105. Simultaneously, an output NQ inverted to 'L' is outputted through the inverter 105, and an output Q inverted to 'H' is outputted through an inverter 106. Subsequently, when the enable signal E becomes 'L' at the time TS2, the TRs 101, 102 are turned off. In this case, 'H' of the G point is inverted by an inverter 3, and supplied as 'H' to an input side of an inverter 104, and 'L' of an H point is supplied as 'H' to an input side of the inverter 103, therefore, even if the TRs 101, 102 are turned off, a level of the H point is held.



LEGAL STATUS

[Date of request for examination] 06.03.1997

[Date of sending the examiner's decision of rejection] 20.10.1998

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to a latch circuit suitable as a means of communication of a high-speed signal.
[0002]
[Description of the Prior Art] Drawing 3 An example of the circuitry of the conventional latch circuit is shown. For an entry-of-data terminal and 307, as for the output terminal of data, and 309, in drawing 3 , the input terminal of an enable signal and 308 are [the memory cell an N-channel metal oxide semiconductor transistor (henceforth NMOSTr) and 303,304 remember an inverter, and as for 305, 301,302 remembers data to be, and 306 / the output terminal of a reversal signal and 310] the input terminals of a reversal enable signal.
[0003] Hereafter, actuation of this latch circuit is explained using drawing 3 and drawing 4 . However, drawing 4 is the timing chart of this latch circuit.
[0004] Data D are inputted from an input terminal 306, and E' which is the reversal signal of enable signal E is inputted from enable signal E and an input terminal 310 from an input terminal 307. If Data D serve as "H" (high level) and enable signal E is reversed "from L" (low)" to H" at the time of day Ts3 just behind that now, NMOSTr301 will turn on, the data of "H" will be incorporated from NMOSTr301, and it will be reversed with an inverter 303. Therefore, the data reversed to "L" are incorporated by G points of the output side of an inverter 303, and it is outputted to them from an output terminal 309. Moreover, "H" is reversed with an inverter 304 and this data of G points is outputted through an output terminal 308.
[0005] Next, if enable signal E is set to "L" at time of day Ts4, since the reversal signal E' becomes "H", NMOSTr301 turns it off and NMOSTr302 turns it on. Since it is reversed with an inverter 304 and "L" level of G points is supplied to F points of the input side of an inverter 303 as "H" level at this time, even if NMOSTr301 turns off, the level of G points is held at "L."
[0006] Moreover, when enable signal E becomes "H", NMOSTr301 turns on and Data D are "L", "H" level is held by same actuation at G points, output-data Q of "L" level is outputted to an output terminal 308, and the output data NQ of "H" level are outputted to an output terminal 309.
[0007] As mentioned above, in the latch circuit shown in drawing 3 , by reversing a signal with an inverter 303, the input data of an input terminal 306 is written in G points, is transmitted in order of inverters 303 and 304, and is outputted from an output terminal 308 as Data Q and data NQ reversed from the output terminal 309.
[0008]
[Problem(s) to be Solved by the Invention] When the data D written in a latch in the latch circuit of the conventional example of drawing 3 are "H" level (namely, VDD), the potential of F points rises only to max (VDD-Vt). VDD is supply voltage and Vt is the threshold electrical potential difference of the NMOS transistor 301 here. On the other hand, when Data D are "L" level, the potential of F points is promptly reduced to 0V. this -- Data D -- " -- the time of being H" level -- the potential of F points -- until -- (VDD-Vt) it is because the electrical potential difference between the gate-sources of the NMOS transistor 301 will descend to a threshold electrical potential difference and a transistor 301 will be in a cut off state, if it reaches. While output voltage becomes large at this time, since equivalent switch resistance becomes large, transfer becomes slow. Although the potential of G points can be pulled up to VDD by preparing the feedback loop of data by the inverter 304 and NMOSTr302 like this example, NMOSTr301 turns off this actuation, and when NMOSTr302 turns on, it is performed for the first time. For this reason, it will be overdue that the potential of G points rises to VDD. Here, when the relation between Vt=Vt0+gamma(Vsb) 1/2 in Vt of NMOSTr301 is according to the substrate bias effectiveness and supply voltage falls, Vt falls, but since it is small if this change is compared with almost all cases at change of supply voltage, the direction of the effect of supply voltage change appears notably. However, Vsb is [the threshold electrical potential difference at the time of Vsb=0 and gamma of the potential difference between the substrate-sources and Vt0] constants. That is, if supply voltage falls, in order that the electrical potential difference built between the gate-sources may decrease, a current decreases, and it becomes late that data are incorporated remarkably to a latch. For this reason, when

the circuitry of a low supply voltage system was designed, high-speed circuit actuation was not attained in the circuit of this configuration.
[0009] Moreover, capacity existed in output wiring which results in an output terminal 308,309, and when this capacity was large, in order to carry out the charge and discharge of this, big delay had arisen. For this reason, it had the problem said that decision of the writing of data becomes slow.
[0010] The purpose of this invention is to offer the latch circuit in which there is little fluctuation of the write-in time amount of data even if it cancels this trouble and supply voltage falls, and a high-speed transfer of the data of both normal rotation and reversal for which write-in time amount does not depend on wiring capacity is possible.
[0011]
[Means for Solving the Problem] In order to attain the above-mentioned purpose, the latch circuit by this invention The inverter for generating the reversal signal of input data, and the memory cell section of a flip-flop configuration with two storage contacts, the 1st and the 2nd, The 1st and the 2nd N-channel metal oxide semiconductor transistor which control the input to said memory cell of the reversal signal generated with the input data and said inverter by the enable signal, It has an inverter for an output for outputting the data held to said memory cell. The normal rotation signal of input data is inputted into said 1st storage contact of said memory cell through said 1st N-channel metal oxide semiconductor transistor. The reversal signal generated with said inverter through said 2nd N-channel metal oxide semiconductor transistor is inputted into said 2nd storage contact of said memory cell. The input of these two signals is controlled by the enable signal to coincidence, and data are outputted through said inverter for an output output at the same time it writes data in said memory cell.
[0012]
[Function] Since the latch circuit concerning this invention uses both input data and its reversal signal for the input to a memory cell as mentioned above, it is lost that the input of another side serves as writing of "L" level even if one input data is the writing of the signal of "H" level, the effect of fluctuation of supply voltage becomes , and write-in time amount becomes extremely long.
[0013] Moreover, definite time amount of data cannot be easily influenced by the capacity of the output wiring section at the time of the writing of data, and the high-speed writing of the data of both normal rotation and reversal is attained.
[0014]
[Example] The latch circuit of one example of this invention is explained below, referring to a drawing. First, drawing 1 shows the circuit diagram of the latch circuit in the example of this invention. In drawing 1 , an inverter for NMOSTr to which 101,102 controls an entry of data by the enable signal, and 108 to generate the reversal signal of data, the memory cell from which 107 constituted the flip-flop with two inverters 103,104, and 105,106 are inverters for an output which are equivalent to the output section of data. Moreover, for the input terminal of an enable signal, and 110, as for the output terminal of a reversal signal, and 112, an entry-of-data terminal and 111 are [109 / the output terminal of data and 113,114] the storage joints of a memory cell 107.
[0015] About the latch circuit constituted as mentioned above, the actuation is explained using drawing 1 and drawing 2 below. However, drawing 2 shows the timing chart in the latch circuit of the example of this invention.
[0016] From an input terminal 110, data D1 are inputted and enable signal E is inputted from an input terminal 109. If data D1 serve as "H" level and enable signal E is reversed "from L"" to H" at time of day Ts1 now, NMOSTr101,102 will turn on and the input data of "H" will be incorporated by G points through NMOSTr101. Moreover, the reversal data D2 reversed by "L" with the inverter 108 are incorporated by H points through NMOSTr102. And the output data NQ reversed through the inverter 105 for an output at "L" to this and coincidence are outputted, and output-data Q reversed to "H" through the inverter 106 for an output is outputted. Next, if enable signal E is set to "L" at time of day Ts2, NMOSTr 101 and 102 turns off. Since it is reversed with an inverter 103, "H" level of G points is supplied to the input side of an inverter 104 as "H" level at this time and "L" level of H points is supplied to the input side of an inverter 103 as "H" level, even if NMOSTr 101 and 102 turns off, the level of G points and H points is held. Even when data D1 are "L", the level of G points and H points is held in the same actuation.
[0017] Thus, the input data inputted from the input terminal 110 is latched for every standup time of day of enable signal E with the reversal signal generated by the inverter 108.
[0018] Here, although the writing of the data of H" level is overdue, it does not become late extremely to be written [input data D1 "is written through NMOSTr101 when it is H" level and supply voltage falls"] in through NMOSTr102, even if supply voltage falls, since it is the signal of "L" level. Moreover, since the input to NMOSTr101 is conversely set to "L" even when the signal written in from NMOSTr102 is "H" level, the write-in time amount of data does not become late. That is, since both reversal signals D2 of input data D1 and D1 are used for the input to a memory cell, even if one input data is the writing of the signal of "H" level, since the input of another side serves as writing of "L" level, the thing with little effect of fluctuation of supply voltage VDD of it which write-in time amount becomes extremely long is lost.

[0019] Moreover, the output section of both the normal rotation signal from a memory cell and a reversal signal is equipped with the inverter for an output, and by designing the size of this inverter in suitable magnitude, it can write in, also when the wiring capacity of the output section becomes large, and fluctuation of time amount can be suppressed. For this reason, even when the wiring capacity of the output section changes, it is not necessary to take into consideration the size of the inverter which constitutes the memory cell section, and it becomes that what is necessary is just to change the size of the inverter of the output section, and the examination course of a circuit constant can be simplified at the time of a circuit design. About the time delay of the data output to wiring capacity, the property of the latch circuit by this example and the conventional latch circuit is shown as compared with drawing 5 R> 5.
[0020] In addition, although the signal of both normal rotation of an input signal and reversal was outputted in this example, this may output only one of signals. In this case, it becomes possible to choose by both of the signals, without changing most configuration of a circuit itself, and easy-ization of a circuit design can be realized.
[0021]
[Effect of the Invention] As mentioned above, according to the latch circuit of this invention, even if supply voltage changes, there is little change of the time amount (time delay) concerning the writing of data, and since the write-in time amount of this data is not dependent on the load-carrying capacity of the output section, it can respond to improvement in the speed of future LSI, and low-battery-ization easily. Moreover, it has the effectiveness of improving the degree of freedom of a circuit design, by latching two data of that the magnitude of the memory cell section can be designed regardless of wiring capacity, normal rotation, and reversal, and being able to output the either.

[Translation done.]